DESIGN OF DIGITAL LOGIC CIRCUITS USING CARBON NANOTUBE FIELD EFFECT TRANSISTORS

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***Abstract*:** The work in this paper plans the essential logic circuits utilizing the carbon nanotube field effect transistor (CNTFET). CNTFET is a novel gadget that is anticipated to outflank scaled CMOS advancements. CNTFET-based gadgets offer high portability for close ballistic transport, high transporter speed for quick exchanging, and also better electrostatic control because of the semi one-dimensional structure of carbon nanotubes. CNTFET uses a semiconducting carbon nanotube (CNT) channel controlled by secluded electrostatic entryways. It shows p-type or n-type exchanging conduct contingent on the extremity entryway voltage. In this paper ambipolar CNTFETs are utilized to structure fundamental logic circuits. The datapath logic squares like half and full-adders are planned and their exhibitions have been researched.

File Terms: Carbon nanotube (CNT), CNT field-effect transistor (CNTFET), Transmission gate (TG), Verilog-AMS.

1. INTRODUCTION

Silicon-based integrated circuit innovation is moving toward its physical farthest point as the gadget measurements scale to the nanometer routine [1]. In the post silicon time, carbon nanotube field effect transistor (CNTFET) is a promising contender for future integrated circuits in light of its incredible properties like close ballistic transport [2], high transporter portability (103– 104 cm2/V•s) in semiconducting carbon nanotube (CNTs) [3, 4], and simple mix of high-k dielectric material bringing about better door electrostatics. CNTs are essentially empty barrels of moved up graphene sheet made out of at least one concentric layers of carbon iotas in a honeycomb cross section course of action. Contingent upon the bearing in which the nanotubes are moved (chirality), they can be either metallic or semiconducting [5]. In a nanotube, low predisposition transport can be about ballistic crosswise over separations of a few hundred nanometer and it is appealing for nanoelectronic applications because of its fantastic electrical properties. The carbon nanotube field-effect transistor consequently as of now accomplished boundless consideration as conceivable option to nanoscale MOS transistor. Because of the comparative I-V attributes of CNTFET as that of MOS gadgets, subjectively the vast majority of the CMOS circuit can be executed utilizing CNTFET [11-13].

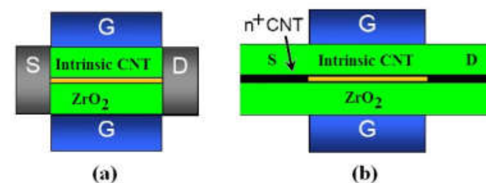


Fig. 1. Different types of CNTFETs: (a) Schottky barrier (SB) CNTFET (b) MOSFET-like CNTFET.

In this work we built up the reduced SPICE good model for CNTFET utilizing Verilog-AMS dialect [14]. The SPICE perfect circuit model of twofold door (D_G) Schottky obstruction (S_B) CNTFET with an ambipolar conduct (n/p-type contingent upon the extremity entryway voltage) [6, 7] is actualized in Verilog-AMS for the circuit recreation of fundamental logic entryways. In the proposed circuits, the logic levels are spoken to as far as voltage esteem considering

adequate clamor edge to keep away from any blunder in calculation. Both static logic and transmission entryway (T_G) based structures are executed and the exhibitions are assessed. The reproduction results indicate astounding execution on power and speed of operation.The rest of the paper is sorted out as pursues. Segment II depicts the basics of ambipolar CNTFETs with uncommon accentuation on circuit good model that we have utilized for our reenactment. Area III depicts the I-V qualities of CNTFET gadgets. The logic door executions utilizing ambipolar CNTFETs and the reenactment results are talked about in Section IV. At last, ends are given in Section V.

2. MODEL FOR CNTFET

CNTs are utilized in the channel district of the CNTFET. Diverse kinds of CNTFET have been shown in the writing. There are for the most part two sorts of CNTFET: Schottky obstruction CNTFET (SB-CNTFET) and MOSFET-like CNTFET as indicated Fig. 1. In SB-CNTFET the channel is made of characteristic semiconducting CNT and direct contacts of the metal with the semiconducting nanotubes are made for source and deplete locales. The gadget chips away at the rule of direct burrowing through the Schottky obstruction (SB) at the source-channel intersection. The boundary width is tweaked by the utilization of entryway voltage, and along these lines, the transconductance of the gadget is controlled by the door voltage. In MOSFET-like CNTFET doped CNTs are utilized for the source and deplete locales and channel is made of inborn semiconducting CNT. A tunable CNTFET with electrical. doping is likewise proposed. It takes a shot at the rule of boundary stature regulation by the utilization of entryway potential. In this work we utilize the S_B-CNTFETs to plan essential logic circuits. Before going into the acknowledgment of the superior computerized circuits utilizing CNTFETs, given us a chance to examine our reproduction display.

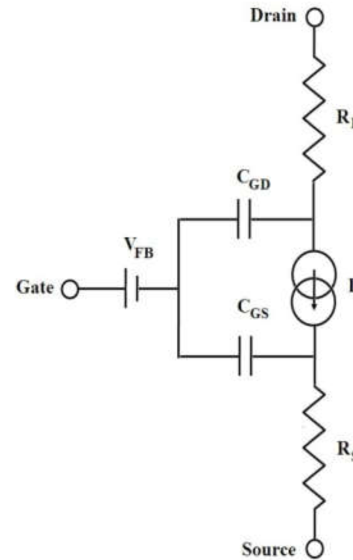


Fig. 2. Schematic of SPICE perfect CNTFET demonstrate, where C_{GS} is door to source capacitance, C_{GD} is entryway to deplete capacitance, R_D is deplete opposition, R_S is source obstruction, V_{FB} is level band voltage, and I_D is deplete current.

First we present the reduced model of twofold entryway (D_G) S_B-CNTFET with am bipolar qualities. We have built up this model in Verilog-AMS utilizing the conservative model which was created at Purdue University [8] (Fig. 2). It is a surface potential-based SPICE perfect model which is utilized to reenact the CNTFETs with ballistic conduct. This model is relevant to a scope of CNTs with distance across between 1 to 3 nm. The computational strategy to assess the deplete current I_D and the aggregate channel charge QCNT is shown in Fig. 3. The principle amounts utilized in the model are the surface potential ΨS and the particular voltage (S/D) that relies upon the surface potential, the subband vitality level Δp and the source (deplete) Fermi level μS/D. The particular voltage is given by

$$\xi_i = \left(\frac{\Psi_S - \Delta_p - \mu_i}{k_B T} \right). \quad (1)$$

For i = source (S), and drain (D). Here, $k_B$is the Boltzmann constant and T is the operating

temperature. When the conduction band minima for the first subband is set to half the nanotube bandgap Δ_1 ($\Delta_1 \approx 0.45$/diameter (in eV)) then the pth equilibrium conduction-band minima Δ_p is given by [9]

$$\Delta_p = \Delta_1 \frac{\left(6p - 3 - (-1)^p\right)}{4} . \quad (2)$$

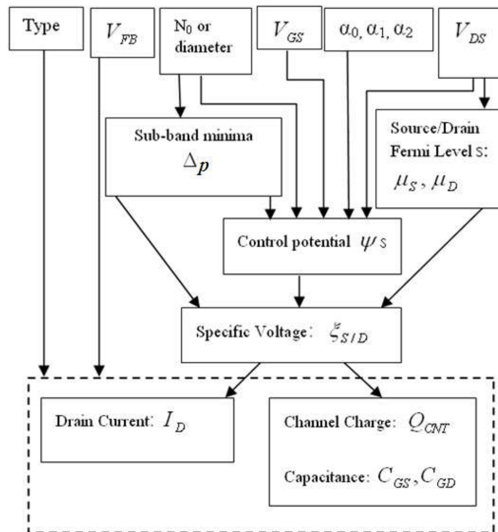


Fig. 3. Structure of CNTFET compact model.

An important step in this model formation is to get the control potential Ψ_S with gate bias voltage. The knowledge of Ψ_S is required to get the specific voltage ξ. This allows us to determine the required output parameter drain current I_D and the total charge Q_{CNT}. In [8] the following approximation is proposed.

$$\begin{aligned} V_{GS} - \psi_S &= 0 && \text{for } V_{GS} < \Delta_1 \\ &= \alpha(V_{GS} - \Delta_1) && \text{for } V_{GS} \geq \Delta_1 \end{aligned} \quad (3)$$

where the parameter α is given by

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2 . \quad (4)$$

Where α_0, α_1 and α_2 are dependent on both CNT diameter and gate oxide thickness [8]. The total drain current I_D is given by [8]

$$I_D = \frac{4ek_BT}{h} \sum_p \left[\ln\left(1 + e^{-\xi_S}\right) - \ln\left(1 + e^{-\xi_D}\right) \right] . \quad (5)$$

Where p is the number of subbands, e is the charge of electron and h is the Planck constant. The gate bias V_G required to produce the assumed Ψ_S based on the electrostatic capacitance given by [8]

$$\psi_S = V_G - \frac{Q_{CNT}}{C_{INS}} . \quad (6)$$

Where C_{INS} is the insulator capacitance. The complete charge relation can be obtained by the sum of charges contributed by all the conduction bands that is populated by drain and source Fermi levels.

So in this way we obtain a simplified SPICE-compatible model of CNTFET and p-type and n-type CNTFET can be obtained by only altering the polarity of the polarity gate (PG) [10]. In the remaining part of the paper we shall use the SPICE compatible model CNTFET for logic circuit realization.

3.I-V CHARACTERISTICS OF CNTFET

The circuit compatible model of SB-CNTFET shown in Fig. 2 has been successfully implemented in Verilog-AMS. At first the p-type and n-type CNTFETs are modelled and simulated in SPICE. The series of *I-V* characteristics of both types of CNTFET (Fig. 4 (a) & (b)) are obtained for 1.5 nm diameter CNT with $R_{S/D} = 75$ kΩ at room temperature (300 K). In order to demonstrate the versatility of this model, we employed it to design basic logic gates. This ambipolar CNTFETs behavior is very similar to the conventional MOSFET. The p-type characteristics are obtained when the polarity-gate voltage is set to 0.2V and the n-type characteristics are obtained when the polarity-gate voltage is set to +0.2V. These ambipolar CNTFETs are used to design circuits replacing the traditional MOS transistors. To perform the simulation of these circuits we arbitrarily decided to use 900 mV power supply and supposed that the flatband voltages are equal to +450 mV and 450 mV for n-type and p-type CNTFETs. The p-type

and n-type characteristics curves shown in Fig. 4 validate the developed model in Verilog-AMS.

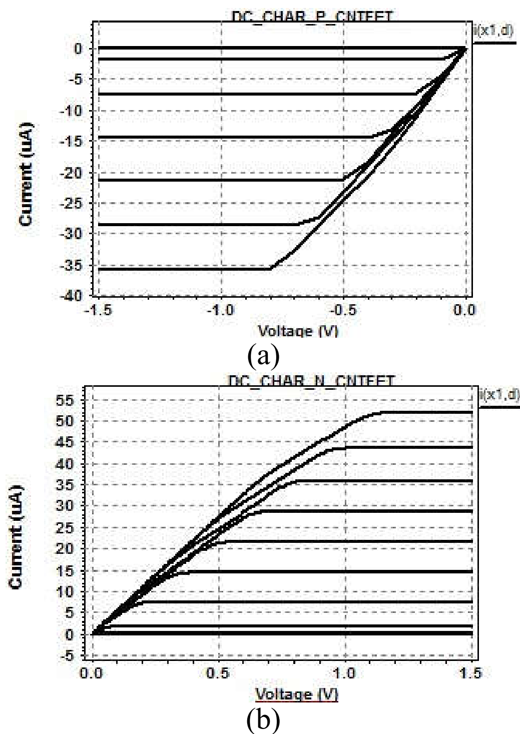


Fig. 4. (a) ID- VDS characteristics of p-type CNTFET. (b) ID-VDS characteristics of n-type CNTFET. Parameters: d = 1.5 nm, RS/D = 75 kΩ, T = 300K.

4. IV.DESIGN AND SIMULATION OF BASIC LOGIC CIRCUITS USING CNTFET

We have designed an inverter circuit as shown in Fig. 5(a) using CNTFET. The pull-up network (PUN) is implemented using p-type CNTFET and the pull-down network (PDN) is implemented using n-type CNTFET. The circuit is simulated in SPICE environment. The CNTFETs with diameter of 1.5 nm, shows very good result. The voltage transfer characteristic of the CNTFET inverter is shown in Fig. 5(b). There is a stiff transition between two states with a threshold voltage equal to half the power supply. The transient simulation result of the inverter circuit is shown in Fig.5(c). The waveforms indicate that there is no logic degradation in both the logic 0 and logic 1 states. The propagation delay through the gate, dynamic power dissipation, and the power delay product (PDP) are calculated which are shown in Table I.

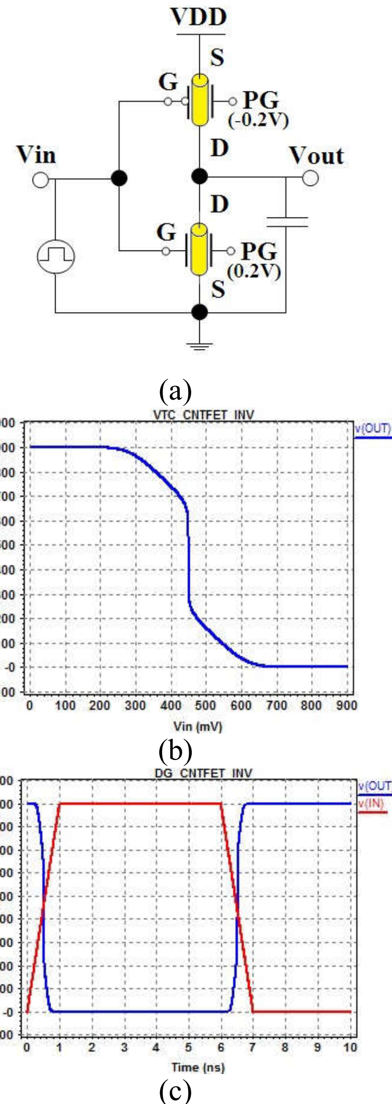


Fig. 5. CNTFET inverter (a) schematic, (b) voltage transfer characteristic, (c) and transient characteristics.

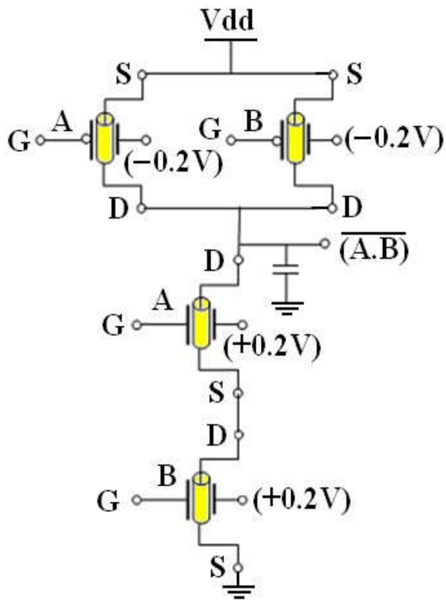


Fig. 6. Two input NAND gate using CNTFET.

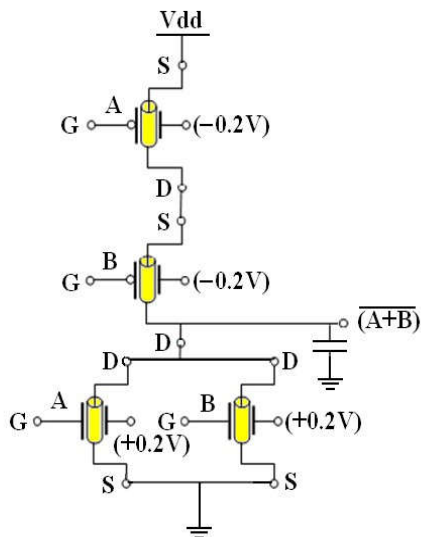
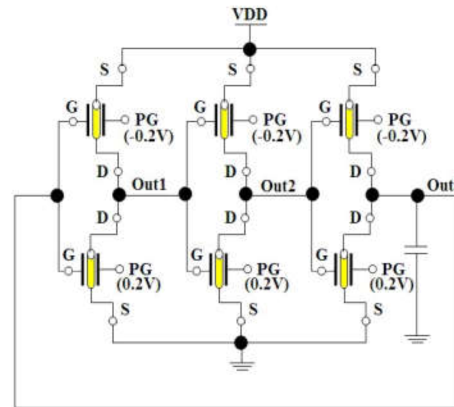
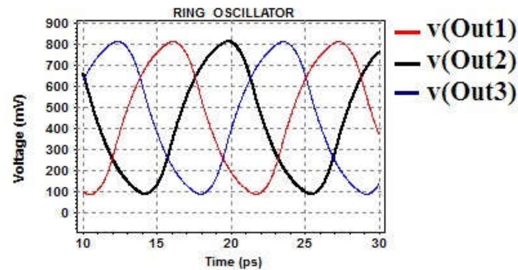


Fig. 7. Two input NOR gate using CNTFET.

Fig. 6 shows the implementation of two-input NAND logic and Fig. 7 shows the implementation of two-input NOR logic circuits. The implementation of the 3-stage ring oscillator is shown in Fig. 8(a). From the transient characteristics shown in Fig. 8(b) the time period (T) of the ring-oscillator is measured as 8.77 ps, which indicates that the frequency of the ring oscillator circuit is 114 GHz.The transmission-gate (TG) is designed using CNTFET in this paper which is analogous to the conventional CMOS-TG. In order to demonstrate the utility of CNTFET-TG based logic, we have employed it to design basic logic gates. In a CNTFET-TG, an n-type and a p-type device are connected in parallel as shown in Fig. 9. This configuration ensures that one of the two transistors restores the signal level in all cases.



(a)



(b)

Fig. 8. 3-stage ring oscillator using CNTFET (a) schematic (b) transient characteristics.

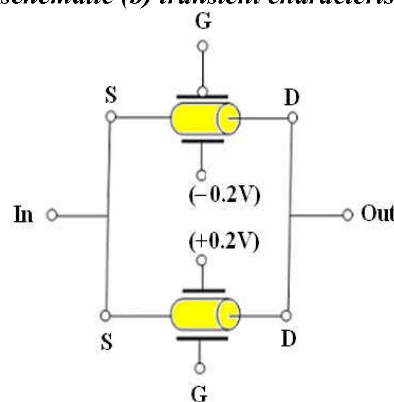
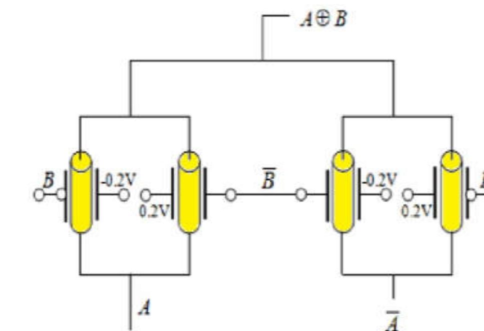


Fig. 9. Transmission-gate using CNTFET.

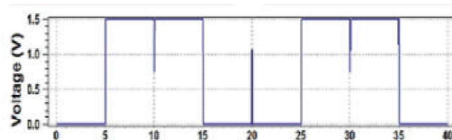
First we demonstrate the XOR logic implemented using CNTFET-TGs as shown in Fig. 10(a). Fig 10(b) shows the transient characteristics of TG XOR. In the XOR logic

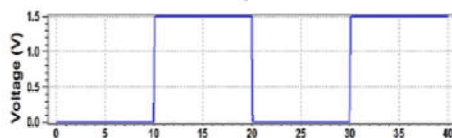
design both the polarities of *A* and *B* are needed. It is possible to implement more functions by utilizing the same configuration just by altering the inputs utilised in the XOR function. For example just by replacing A by I_0 and complement of A by I_1 we can implement the 2:1 multiplexer. The TG is the first step toward the reconfigurable logic design, i.e. by changing the inputs only the same configuration can result different Boolean functions.

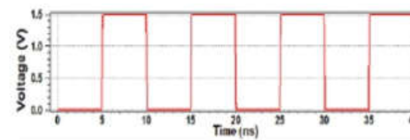
Next we have designed the half-adder, and full-adder using static CNTFET logic and CNTFET-TG logic. The designs are simulated in the SPICE environment to characterize their performances in terms of power dissipation and delay. The CNTFET-TG based designs show excellent power and delay performance than the ambipolar static CNTFET logic families. The delay, power, and PDP for different logic circuits are



(a)







(b)

Fig. 10. (a) TG XOR using CNTFET, (b) transient characteristics of CNTFET TG XOR.

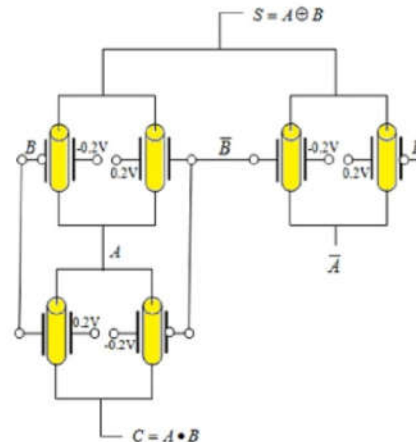


Fig. 11. Half-adder using CNTFET-TG.

Shown in table I and II. The results show that CNTFET-TG based logic is much superior than the static CNTFET based logic.

TABLE I: AVERAGE DELAY, POWER, AND POWER-DELAY-PRODUCT (PDP) FOR CNTFET BASED DESIGNS.

Logic block	Power (J/s) (×1e-7)	Delay (s) (×1e-9)	PDP (J) (×1e-16)
Inverter	1.80	2.52	4.53
NAND	1.84	2.58	4.74
NOR	1.82	2.54	4.63
XOR	2.10	2.58	5.41
Half-adder	2.82	6.00	16.92
Full-adder	3.21	7.09	22.76
Transmission Gate Inverter	1.40	2.24	3.14

TABLE II: AVERAGEDELAY, POWER, AND POWER-DELAY PRODUCT OF TG-XOR, TG-HALF-ADDER AND TG-FULL-ADDER

Logic block	CNTFET-TG based logic		
	Power (J/s) $(\times 10^{-7})$	Delay (s) $(\times 10^{-9})$	PDP (J) $(\times 10^{-16})$
TG XOR	1.62	1.96	3.18
TG Half-Adder	1.9	4.6	8.74
TG Full-Adder	2.4	6.2	14.8

V.CONCLUSION

In this paper we have built up a SPICE good model for carbon nanotube field-effect transistor utilizing Verilog-AMS. The model is utilized to structure static logic circuits, transmission entryway based logic circuits and datapath logic circuits like half-viper, and full-snake. The exhibitions are contemplated regarding force, deferral, and PDP. The CNTFET-TG based logic circuits indicate fantastic power and postpone results when contrasted with that of CNTFET based static logic circuits. The model gives an integrated structure to help SPICE based CNTFET circuit plan and recreation. The CMOS and CNTFET co-plan and reproduction are additionally empowered with this model.

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