

# Performance investigation of Cascade H-Bridge MLI Fed with IM Drive

D.Vinoth<sup>1</sup>, C.Nagarajan<sup>2</sup>, Badmanaban C<sup>3</sup>, Boobeshkannan P<sup>4</sup>, Sekar M<sup>5</sup>

<sup>1</sup> Asst.Professr, <sup>2</sup> Professor and Head, <sup>3,4,5</sup> UG Students ,Department of Electrical and Electronics Engineering, Muthayammal College of Engineering

**Abstract**— This paper presents a three phase fifteen level cascaded H-bridge (CHB) multilevel inverter for open end stator winding induction motor drive system. An inverted sine PWM method is used to achieve minimum total harmonics distortion (THD) in the output voltage of multilevel inverters. The analysis of the output voltage harmonics are carried out and compared with the nine level conventional cascaded H-bridge inverters. The proposed system is verified through simulation and the simulation results are compared with the conventional inverter. From the result the proposed inverter offers much less total harmonic distortion.

**Index Terms**—H-bridge, PWM, harmonic distortion, cascaded multilevel inverter

## I. INTRODUCTION

Power electronic converters, especially dc/ac PWM converters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance and so on.

For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors and so on. As a cost effective solution, multilevel converter not only achieves high power ratings, but also enables the use of low power application in renewable energy sources such as photovoltaic, wind and fuel cells which can be easily interfaced to a multilevel converter system for a high power application.

The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters. More recent applications have been for power system converters for VAR compensation and stability enhancement, active filtering, high-voltage motor drive, high-voltage dc transmission and most recently for medium voltage induction motor variable speed drives. Many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, Flexible AC Transmission System (FACTS) and traction drive systems.

In recent years, multilevel inverters have received more attention in industrial applications, such as motor drives, static VAR compensators and renewable energy systems. Compared to the traditional two-level voltage source inverters, the stepwise output voltage is the major advantage of multilevel inverters. This advantage results in higher power quality, better electromagnetic compatibility, lower switching losses, higher voltage capability, and needlessness of a transformer at distribution voltage level, thereby reducing the costs. In all the cases, the output voltage contains distortions. A new fifteen-level inverter topology, consisting of conventional three-phase two-level voltage source inverters powered by isolated dc sources and floating-capacitor-connected H-bridges, has been presented. In this paper, the inverted sine PWM based control scheme is used, and it is capable of balancing the asymmetrical-bridge capacitor voltages, in the entire modulation range, at any power factor, under transient as well as steady-state operating conditions.

## II. CONVENTIONAL TOPOLOGY

In the existing system, the prototype considered the order of 9-level cascaded type multilevel inverter. In this project, a new scheme for nine-level voltage space-vector generation for medium-voltage induction motor (IM) drives with open-end stator winding is presented. Its ability to operate in 5-level or 3-level mode, in case of any failure in the H-bridges. This feature enhances the reliability of the proposed drive system.

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The neutral point converter proposed by Nabae, Takahashi and Akagi in 1981 was essentially a three-level diode-clamped inverter.

A three-level diode clamped inverter consists of two pairs of switches and two diodes. Each switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. In a three-level inverter each of the three phases of the inverter shares a common dc bus, which has been subdivided by two capacitors into three levels. The DC bus voltage is split into three voltage levels by using two series connections of DC capacitors,  $C_1$  and  $C_2$ . The voltage stress across each switching device is limited to  $V_{dc}$  through the clamping diodes  $D_{c1}$  and  $D_{c2}$ . It is assumed that the total dc link voltage is  $V_{dc}$  and mid point is regulated at half of the dc link voltage, the voltage across each capacitor is  $V_{dc}/2$  ( $V_{c1}=V_{c2}=V_{dc}/2$ ).

In a three level diode clamped inverter, there are three different possible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. For a three-level inverter, a set of two switches is on at any given time and in a five-level inverter, a set of four switches is on at any given time and so on. Fig-2.1 shows the circuit for a diode clamped inverter for a three-level and a five-level inverter.

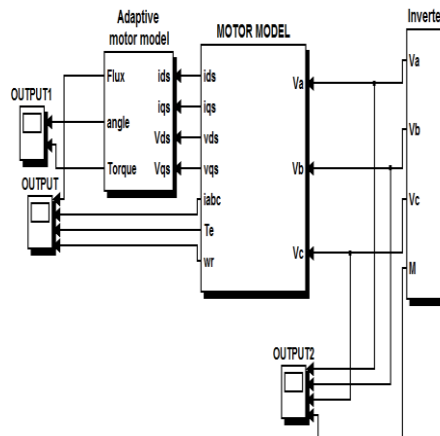


Fig.2.1. Simulation diagram for 9- level cascaded MLI.

The Fig.2.2 shows the phase voltage and line voltage of the three-level inverter in the balanced condition. The line voltage  $V_{ab}$  consists of a phase-leg a voltage and a phase-leg b voltage. The resulting line voltage is a 5-level staircase waveform for three-level inverter and 9-level staircase waveform for a five-level inverter. This means that an N-level diode-clamped inverter has an N-level output phase voltage and a  $(2N-1)$  level output line voltage.

In general the voltage across each capacitor for an N level diode clamped inverter at steady state is  $V_{dc}/(N-1)$ . Although each active switching device is required to block only a voltage level of  $V_{dc}$ , the clamping diodes require different ratings for reversevoltageblocking.

In general for an N level diode clamped inverter, for each leg  $2(N-1)$  switching devices,  $(N-1) * (N-2)$  clamping diodes and  $(N-1)$  dc link capacitors are required. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. However, capacitor voltage balancing will be the critical issue in high level inverters. When 'N' is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge. Though the structure is more complicated than the two-level inverter, the operation is straightforward.

## III. PROPOSED SYSTEM

In proposed system, the prototype is altered to inverted sine PWM and the order is get extended from 9- level fig 3.1 and 15- level fig 3.2. In this project demonstrates reduced harmonic distortion can be achieved for a new topology of multilevel inverters with inverted sine PWM. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter and can be extended to any number of levels.

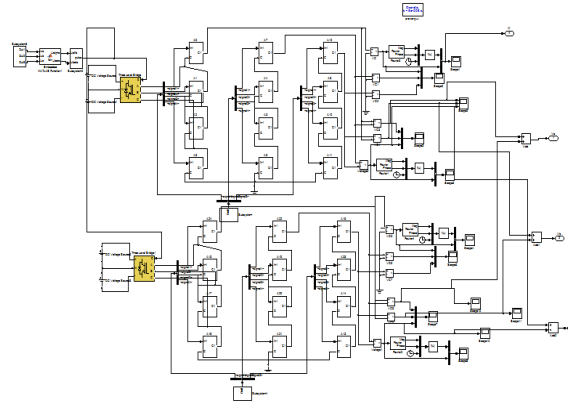


Fig.3.1. 9- level Inverter Simulation Diagram.

The inverted sine carrier PWM (ISPWM) method uses the conventional sinusoidal reference signal and an inverted sine carrier. The control strategy uses the same reference (synchronized sinusoidal signal) as the conventional SPWM while the carrier triangle is a modified one. The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. In the gating pulse generation of the proposed ISCPWM scheme, the triangular carrier waveform of SPWM is replaced by an inverted sine waveform. For an 'm' level inverter, (m-1) carrier waves are required. The pulses are generated when the amplitude of the modulating signal is greater than that of the carrier signal. The proposed control strategy has a better spectral quality and a higher fundamental output voltage without any pulse dropping.

The advantages of ISPWM method are it has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM (SPWM) without any pulse dropping. The ISCPWM strategy enhances the fundamental output voltage particularly at lower modulation index ranges. There is a reduction in the total harmonic distortion (THD) and switching losses. To increase the fundamental amplitude in the sinusoidal pulse-width modulation the only way is by increasing the modulation index beyond 1 which is called over modulation. Over modulation causes the output voltage to contain many lower order harmonics and also makes the fundamental component vs. modulation index relation non-linear.

Inverted sine pulse width modulation technique replaces over modulation. The appreciable improvement in the total harmonic distortion in the lower range of modulation index attracts drive applications where low speed operation is required. ISPWM technique causes marginal increase in the lower order harmonics, but except third harmonic all other harmonics are in acceptable level. But for three phase applications the heightened third harmonics need not be bothered.

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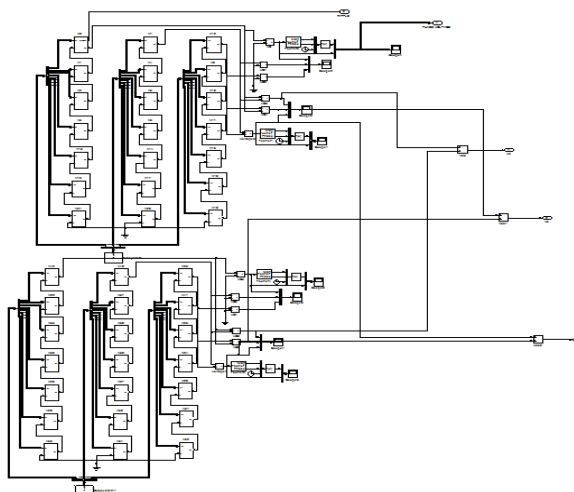


Fig.3 2. Fifteen-level Inverter Simulation Diagram

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IV. SIMULATION RESULTS

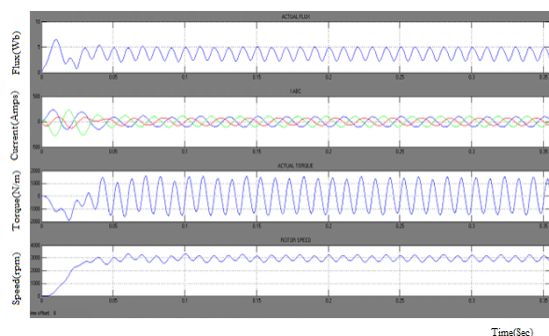


Fig 4.1 Nine- Level Cascaded MLI Output

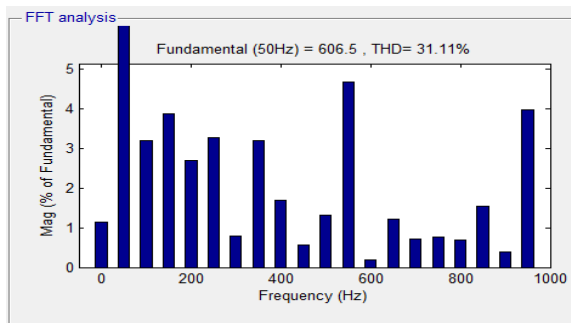


Fig 4.2 THD value for conventional inverter

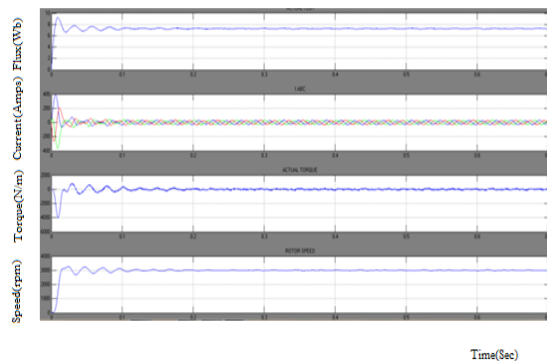


Fig 4.3 Fifteen- Level Cascaded MLI Output

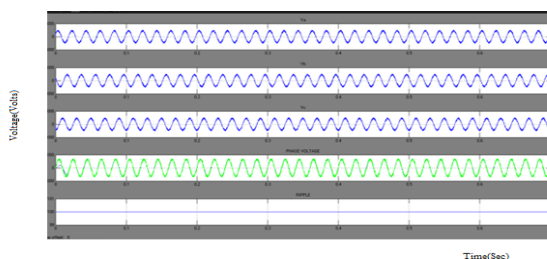


Fig 4.4 Fifteen - level Inverter Output

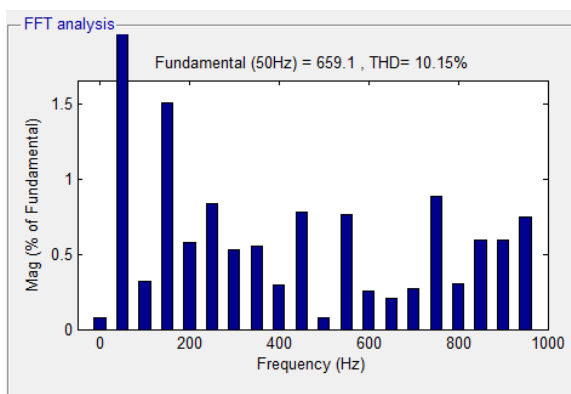


Fig 4.5 THD value for proposed inverter

V. CONCLUSION

A new basic multilevel module (MLM) for the multilevel converter has been proposed. The proposed topology is a combination of MLMs and full-bridges converter. The proposed topology extends the design flexibility and the possibilities to optimize the converter for various objectives. It has been shown that the structure, consisting of MLMs with to switches has the minimum number of

switches for a given number of voltage levels. It has been shown that the proposed topology provides 15 levels on the output voltage. The proposed topology not only has lower switches and components in comparison with other one, but also its full bridge converters operate in the lower voltage. Reduction of the power losses of the proposed topology is another advantage of the proposed converter. The proposed topology can be a good solution for applications that require high power quality, or applications that have considerable numbers of dc voltage sources. The simulation for the existing and proposed was done by using the MATLAB/Simulink. The various voltage and current waveforms are also verified. In future the increased levels in the cascaded multilevel inverter for open-ended stator winding will be done and the simulation results for various voltage and currents also have to be verified.

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