HIGH SPEED SYNCHRONIZATION OF ON-CHIP INTERCONNECT TRANSCEIVER USING MIXED DELAY LOCKED LOOP

[1]A.NAGA GANESH, [2]M.BHASKAR

[1]A.Naga Ganesh, Assistant professor, Dept. of ECE, Vishnu Institute of Technology, Bhimavaram, India

[2]M.Bhaskar, Professor, Dept. of ECE, National Institute of technology(NIT), Tiruchirappally, India

ABSTRACT: In this paper a novel architecture for a DLL is presented. DLL circuit contains, phase detector, charge pump and voltage controlled delay line (VCDL) blocks.

Phase detector compares the phase information, modified and implemented with least hardware with optimum metric. A loop filter as charge pump perceives phase error information and sends corresponding charge to VCDL. Current starved inverters used in VCDL. In this thesis, the sizes of the transistors are determined, using the method of logical effort for various frequencies of operation and the simulations are carried out. The proposed DLL is implemented in UMC 0.09µm technology and post layout simulations are carried out in CADENCE SPECTRE Tool. From the simulation it is observed that the mixed DLL operates in the frequency range of 650MHz to 3GHz with a locking period of two clocks and has a jitter of approximately 2.3ps.

KEY WORDS: Delay-locked loop, mixed-mode, fast locking, phase, low power.

I.INTRODUCTION

Nowadays, DLLs and PLL (Phase locked loop) s are widely used in memory devices, high-speed microprocessors and communication integrated circuits. In these applications, the signal skews and jitters are removed using the DLL or PLL for high-speed signaling. PLL has the advantage of providing the input frequency at various output frequencies. However, the PLL suffers from long locking time. more stable, easier to implement with digital circuits and provide better jitter performance. Generally, if no frequency multiplication is required, DLLs are more attractive than PLLs because they are more stable and easier to implement with digital circuits. They also exhibit better jitter accumulation characteristics than PLLs.

DLLs can generally be classified into three types: analog, digital, and mixed mode. Analog DLL have better skew and jitter. However, it is not widely used these days because of analog DLL process variability, which is more affected and has a high degree of integration due to long locking time and large area. As an alternative to these analog DLLs, Mixed DLLs can be easily shrunk and have a faster locking time. A closed-loop Mixed DLL has the fastest locking time and low power consumption.

In the coarse lock step, the frequency range is selected by Logical effort method to improve time resolution. Based on the narrowed frequency range, the VCDL (voltage control delay line) is adjusted with an analog feedback loop that is a fine step to provide relatively fast lock times. Mixed-mode DLLs offer low jitter by implementing precise digital and analog control and the advantage of being able to compensate for PVT variations. A high-performance DLL with both low jitter and fast locking time is required. Low-jitter is provided using a coarse-grained Logical effort scheme. To achieve fast lock times versus conventional DLL, we propose a mixed-mode DLL, uses current starved inverters.

Conventional DLLs may suffer from harmonic locking over a wide operating frequency range. Therefore, various wide-range DLLs architectures have been developed to solve the false locking problem... In, an all-analog DLL uses the replica delay line to solve the narrow operating frequency-range problem of a conventional DLL. However, the analog DLLs are more strongly affected by the process variation. Therefore, Mixed DLLs is developed to improve process portability. In the all-mixed multiphase clock generator is used to overcome the false locking problem. In phase detector the phase error information obtained by reference clock and the output clock signal.

II. EXISTED SYSTEM

This architecture of multi-phase mixed DLL used for the serial link is given Fig.1. It consists of Phase comparator, which compares the phase of reference Clk with the final output of the VCDL. UP or DOWN pulse is generated when Clk signal leads or lags the final output respectively. The Fig.1 shows the block architecture of existed system. Basically, it requires two input signals as shown in figure (1). This UP or DOWN pulse is given to the Charge pump where corresponding control voltage V_{ctrl} is produced. The purpose of VCDL is to produce 4 clock signals of equal phase shift. The VCDL takes V_{ctrl} as input and adjusts the phase of these signals corresponding to the voltage being fed. Thus, the output of DLL aligns with the reference input after few clock cycles.

DLLs have been used for clock distribution circuits, multiphase clock generation and clock recovery circuits.

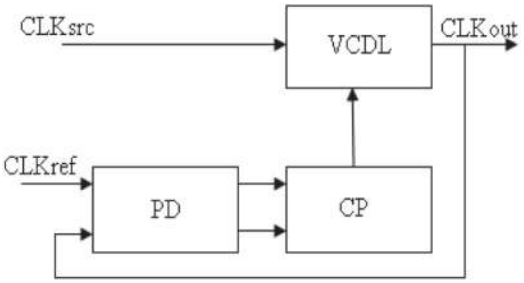

Fig. 1. Existed system

The current-starved inverter is used to adapt the delay in fair manner. In this the delay line receives a reference clock signal and passes it through a series of delay line taps. Phase adjustment is performed by voltage controlled delay line. Each tap provides a signal adjacent in phase to the signal at its neighboring taps. The length of the delay line depends on the frequency of the input data and the inverter delay. The physical layout of existed system is shown in below figure (2).

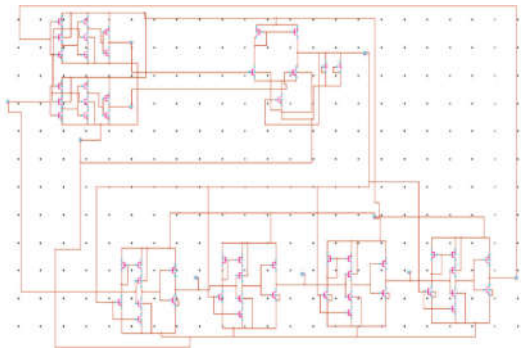

Fig. 2. Layout of Existed system

This system works up to 1.25 GHz However, this method is accompanied by a large area that is suffering from long-term dead time, large power loss, production of analogue intensive, large-capacity and extensive calibration required. In the same time resolution of the circuit increases, due to this delay increases. To decrease the delay occurred in the system a new system is proposed which is discussed in below section.

III. PROPOSED SYSTEM

The purpose of this DLL is to provide an output clock signal very close in phase to the data edges. The main feature of proposed design is to implement output clock locked with reference clock in less time and low jitter at high frequencies. The idea is based on inverter operation in which either reference or output clock is connected in the place of power supply to extract phase error information as up and down pulses. Reduces the transistor count from eight to two for each phase detector. The Charge pump is approximated as two switches. The two switches are controlled by the up pulses and the down pulses, respectively. Once the switch is closed, the current source or sink will start adding charge onto or removing charge from the loop filter (capacitor). This charging or discharging process will continue until lock is achieved. In the locked state, the voltage (charge) of the loop filter is kept constant.

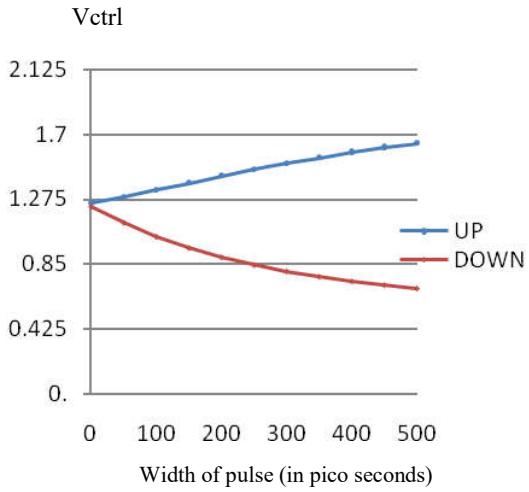

Fig. 3 Response curve of charge pump

A VCDL based on current starved inverter is used in our implementation. The loading problem is occurring due to control voltage is being given to source terminal of each stage of VCDL line and compensated.

The figure (4) shows the physical layout of proposed system.

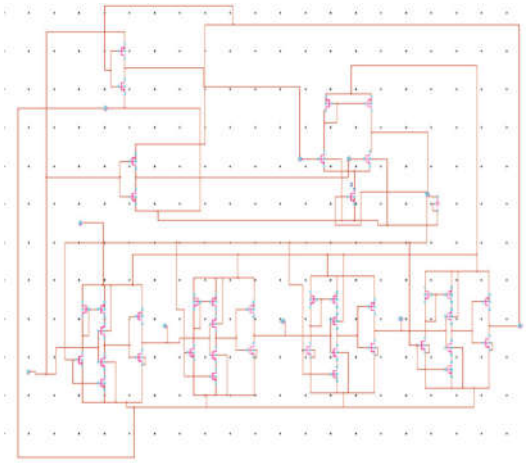

Fig. 4. Layout of Proposed system

Our proposed DLL scheme can be implemented simply with the assistance of reference clock, having smaller area and low power consumption. Due to the coarse step, the voltage range to be controlled can be reduced due to the narrowed time resolution in the analog loop, which is a fine step. Since the phase out clock must cover both the fast and slow states relative to the reference clock, charge the initial state of the capacitor of the loop filter to half of supply voltage and finish the analog step at a fast lock time. Therefore, the maximum correction time of the proposed DLL is within less number of clock cycles. From below table 1 we can observe the performance comparison of existed and proposed system.

S.No.	Specification	Proposed System	Existed System
1	Locking Time	4	6
2	Jitter	~2.3 ps@2.8GHz	~8ps@1.2GHz
3	Operating Frequency	0.65 – 3GHz	0.65 – 1.25GHz
4	Transistor Count in Phase Detector	2	8
5	Transistor Count in Charge Pump	5	7

Table. 1. Performance comparison

The figure(5) shows the output of proposed system.

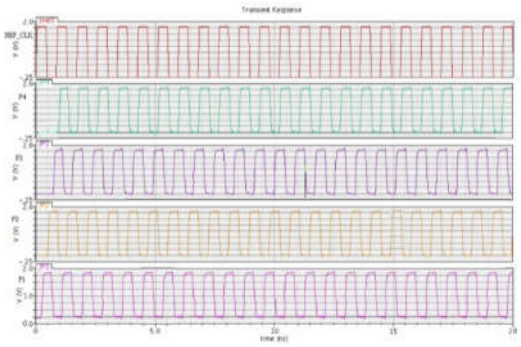

Fig. 5. Output waveform of proposed system

IV. CONCLUSION

The DLL proposed in this paper provides fast lock time, high accuracy and low power consumption. To achieve these, we have a simple technique of Mixed DLL with phase difference in the first coarse step, which improves the coarse step time resolution without much additional lock time. The coarse tune circuit is proposed to reduce the lock time and keep a better jitter performance in this DLL. The charge pump circuit is implemented by the loop filter to achieve adaptive bandwidth. Consequently, this DLL can operate correctly when the input clock frequency is changed.

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