# Design of Multilevel HAAR Wavelets for High-throughput Computation of VLSI Architectures

**K.Divya*, J.Gayathri**, K.Rajalakshmi*****
* Assistant Professor ** Assistant Professor
Department of Electronics & Communication Engineering,
*Prince Dr. K. Vasudevan College of Engineering and Technology, Tamil Nadu, India
**Prince Shri Venkateshwara Padmavathy Engineering College,Chennai
***Faculty, Prince Shri Venkateshwara Arts and Science College, Gowriwakkam

*Abstract*— ***The scalable and pipeline architecture as well as the parallel transformation for the high-throughput computation is performed using the Haar wavelets transform. In this paper, both lossy and lossless compression can be predicted by the wavelets and it is also used for both low and high value data efficiency. As compared to the Haar wavelet, we generate a high precision for an image instead of using a Daubechies wavelet transform. An emerging and efficient method for imaging, sorting, coding and compression processes is the distinct dimension of the Haar wavelet.. The transformation of the Aar wavelet enables an image to be coded according to the level of detail and supports theoretical results of formulation and simulation, and it is important to transmit data through the compression technique in a safe way. We have to be implemented in an FPGA for low and cost implementation to see other possibilities for using the proposed high throughput structure.***

*Keywords*— ***Daubechies wavelet, high-throughput, Haar wavelet, compression technique.***

## I.Introduction

This The DWT can be divided into two categories: lossy and lossless DWT. The lossy DWT is mainly used in situations that demand a high compression ratio; thus, it is very appealing in military, HD satellite images, motion detection, network distribution and storage purposes. On the other hand lossless transformation is used in medical imaging, digital negative (DNG) and some digital cameras for compressing the images. But as the coefficients of the lossy filter are real floating point numbers, the computational complexity of implementation is very high. Moreover, the lossy transform is irreversible, i.e. there is some loss in the image during this transformation. For lossless DWT, the amount of compression is considerably less compared to that of lossy DWT.

Using lossless DWT, which is a requirement in medical imaging, infinite PSNR will preferably be achieved. In applications such as satellite imaging systems, multi-spectral imaging and tele-medicine systems, all forms of compression are required for lossy and lossless, where less relevant data and image thumbnails can be compressed using lossless DWT and high-resolution images and medical data can be compressed. Satellite image enhancement is the most frequently used technique in the field of image processing to improve feature visualization. In many image processing applications such as image compression, bio-informatics, the DWT is a significant operation. Standardized in forms such as JPEG 2000, the DWT has many desirable characteristics, such as the absence of artefact blocking, higher resolution capacity, computation in place, and better peak signal to noise ratio (PSNR) etc. Today, a large number of volumetric image data sets are created by many medical imaging systems, such as computed tomography (CT), positron emission tomography (PET), and magnetic resonance imaging (MRI). Many modern apps need to process these datasets with various resolutions and features online or offline (region of interests, scaling, etc.). All these specifications listed above for 2-D images are protected by Part 1 and Part 2 of the JPEG 2000 standard.

For JP3D, the simple transform algorithm is 3-D DWT. It is a powerful video coding sub-module, like Motion-JPEG, which is shown to be more reliable than the standard MPEG-4. The emergence of 3-D and 4-D medical imaging systems has intensified the need for a 3-D compression method for volumetric images. 3-D DWT processing of 3-D magnetic resonance (MR) brain images to remove features for Alzheimer's disease diagnosis and mild cognitive impairment in subjects.

## II. BACKGROUND AND RELATED WORK

### HAAR WAVELET

The Haar wavelet is a sequence of rescaled' square-shaped' functions in mathematics that forms a wavelet family or basis. Wavelet analysis is analogous to Fourier analysis in that it requires an orthonormal basis to describe a target function over an interval. As the first known wavelet basis, the Haar sequence is recognized and used extensively as a teaching example. Alfréd Haar suggested the Haar series in 1909. To give an example of an orthonormal system for the space of square-integrated functions in the unit interval, Haar used these functions [0, 1]. Not until much later did the analysis of wavelets arrive, and even the word "wavelet." As a special Daubech case, As a special case of the Daubechies wavelet, the Haar wavelet is also known as Db1. The Haar Wavelet is also the simplest wavelet possible. The technological drawback of the Haar wavelet is that it is not continuous, so it cannot be distinguished. However, for the study of signals with abrupt transitions, such as monitoring of instrument failure in devices, this property may be an advantage.

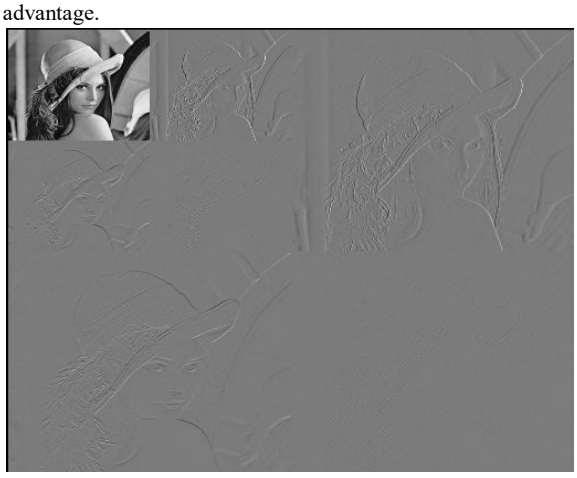


**Fig 1**:Haar transform wavelet

Two iteration of 2D Haar Wavelet decomposition on the lenna image. The original image is high-pass filtered, yielding the three detail coefficients sub-images (top right: horizontal, bottom left: vertical, and bottom right: diagonal). It is then low-pass filtered and downscaled, yielding an approximation coefficients sub image (top left); the filtering process is repeated once again on this approximation image.

In mathematics, the Haar wavelet is a certain sequence of functions. It is now recognized as the first known wavelet. This sequence was proposed in 1909 by Alfred Haar. Haar used these functions to give an example of a countable orthonormal system for the space of square integrable functions on the real line. The study of wavelets, and even the term "wavelet", did not come until much later. The Haar wavelet is also the simplest possible wavelet. The technical disadvantage of the Haar wavelet is that it is not continuous, and therefore not differentiable.

The Haar wavelet's mother wavelet function ψ(t) can be described as

$$\psi(t) = \begin{cases} 1 & 0 \le t < 1/2, \\ -1 & 1/2 \le t < 1, \\ 0 & \text{otherwise.} \end{cases}$$

and its scaling function φ(t) can be described as

$$\phi(t) = \begin{cases} 1 & 0 \le t < 1, \\ 0 & \text{otherwise.} \end{cases}$$

All Wavelets are mathematical functions that were developed by scientists working in several different fields for the purpose of sorting data by frequency. Translated data can then be sorted at a resolution which matches its scale. Studying data at different levels allows for the development of a more complete picture. Both small features and large features are discernable because they are studied separately. Unlike the discrete cosine transform, the wavelet transform is not Fourier-based and therefore wavelets do a better job of handling discontinuities in data. The Haar wavelet operates on data by calculating the sums and differences of adjacent elements. The Haar wavelet operates first on adjacent horizontal elements and then on adjacent vertical elements.

The Haar transform is computed using

$$\frac{1}{\sqrt{2}}\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}.$$

## III.PROPOSED METHODOLOGY

**BLOCK DIAGRAM**:

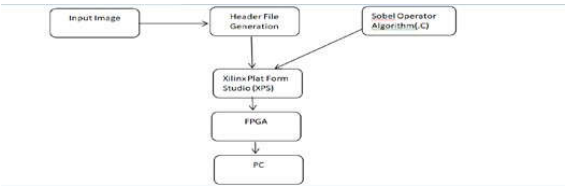
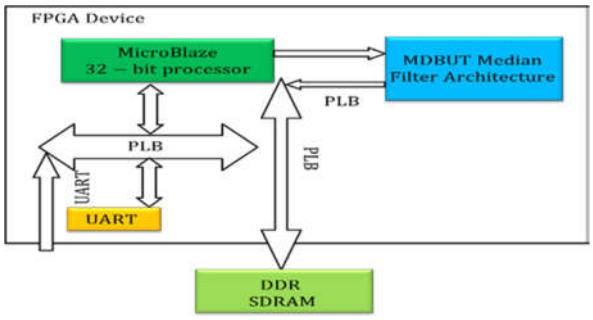



**Fig 2**: Block diagram

**DESIGN:**

Inside Xilinx FPGA for System-on-a-Chip (SOC) processors, there are different ways to include processors: PowerPC hard processor core, or Xilinx Micro Blaze soft processor core, or VHDL/Verilog user-defined soft processor core. In this job, due to the versatility, the 32-bit Micro Blaze processor is selected. Based on the hardware budget, the user can customize the processor with or without advanced features. Memory management unit, floating processing unit, hardware multiplier, hardware divider, instruction and data cache links are included in the advance features, etc. The system's design description is shown in Figure 2. Two separate buses (i.e. the processor local bus (PLB) and the fast simplex connection (FSL bus) are used in the system[5-6]) can be seen. PLB follows the IBM core link bus architecture, which supports up to 128-bit data bus, up to 64-bit address bus and centralized bus arbitration for high bandwidth master and slave devices. It is a type of shared bus service.. Besides the access overhead, PLB potentially has the risk of hardware/software incoherent due to bus arbitration. On the other hand, FSL supports point-to-point unidirectional communication. A pair of FSL buses (from processor to peripheral and from peripheral to processor) can, without an arbitration mechanism, form a dedicated high-speed bus. For easy access, Xilinx provides C and assembly language support. Most peripherals are therefore linked via PLB to the processor; instead, the DWT coprocessor is connected via FSL.

**Fig 3**: System Overview




Several methods for the distribution of data are given by the current framework. These methods are regulated by UART, VGA, and Ethernet. The UART is used to provide a host computer with an interface, to enable user interaction with the device and to facilitate data transfer. A standalone real-time display is created by the VGA centre. The Ethernet link provides a simple way to export data to other networks for use and study. In our job, an image data stream is generated using Visual Basic to validate the DWT coprocessor, then transmitted from the host device to the FPGA board via the UART port.

In terms of its instruction-set architecture, Micro Blaze is very similar to the RISC-based DLX architecture described in a popular computer architecture book by Patterson and Hennessy. With few exceptions, the Micro Blaze can issue a new instruction every cycle, maintaining single-cycle throughput under most circumstances

The Micro Blaze has a versatile interconnect system to support a variety of embedded applications. Micro Blaze's primary I/O bus, the Core Connect PLB bus, is a traditional system-memory mapped transaction bus with master/slave capability. A newer version of the Micro Blaze, supported in both Spartan-6 and Virtex-6 implementations, as well as the 7-Series, supports the AXI specification. The majority of vendor-supplied and third-party IP interface to PLB directly (or through an PLB to OPB bus bridge.) For access to local-memory (FPGA BRAM), Micro Blaze uses a dedicated LMB bus, which reduces loading on the other buses. User-defined coprocessors are supported through a dedicated FIFO-style connection called FSL (Fast Simplex Link). The coprocessor(s) interface can accelerate computationally intensive algorithms by offloading parts or the entirety of the computation to a user-designed hardware module.

The Micro Blaze processor is a 32-bit Harvard Reduced Instruction Set Computer (RISC) architecture designed for Xilinx FPGA implementation with separate 32-bit instruction and data buses operating at full speed to simultaneously execute programmes and access data from both on-chip and external memory. The architecture's backbone is a single-issue, 3-stage pipeline with 32 general-purpose registers (no address registers like the Motorola 68000 Processor are available), an Arithmetic Logic Unit (ALU), a shift unit, and two interrupt stages.

This basic design can then be configured to conform to the exact needs of the target embedded application with more advanced features such as: barrel shifter, divider, multiplier, single accuracy floating point unit (FPU), instruction and data caches, exception handling, debug logic, interfaces with Fast Simplex Connection (FSL) and others. This versatility allows the user to balance the output expected by the target application against the expense of the soft processor's logic region. The white items are the core of the Micro Blaze architecture, while the shaded grey items are optional features that are available depending on the exact specifications of the embedded target programme. The Micro Blaze is a virtual microprocessor that is built by combining blocks of code called cores. Micro Blaze is an embedded soft core that includes the following feature.

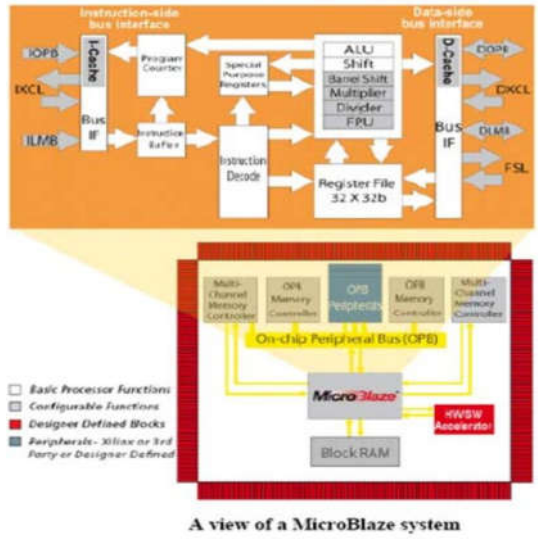
• Thirty-two 32-bit general purpose registers.

• 32 bit instruction word with three operands and two addressing modes.

• Separate 32-bit instruction and data buses that conform to IBM's OPB (On-chip Peripheral Bus) specification.

• 32-bit address bus

• Single issue pipeline




**A view of a MicroBlaze system**

**Fig 4**:Micro Blaze system

## IV.RESULTS AND DISCUSSIONS

### *HAAR WAVELET TRANSFORM*

A fair amount of work is therefore a measurement of a wavelet coefficients at any possible size, and it produces a terrible amount of data. If the scales and location are selected, the so-called dyadic scales and positions are centred on the power of two, then wavelet coefficients are determined and just as precise. This is obtained from the transformation of the Haar wavelet (HWT). The provided input image is converted to pixel values in the mat lab section 1 during pre-processing.

### EXTRACTION PROCESS

In the previous chapters, the Haar wavelet transform method and the built architecture for the necessary functionality were discussed. This chapter now deals with the HWT process's simulation and synthesis performance. The test bench is designed to test the functionality of the model. This established test bench will force the inputs automatically and will perform the algorithm's operations.

## V. CONCLUSION AND FUTURE ENHANCEMENT

In this a haar wavelet transform presented an approach towards VLSI implementation of the compression. This can be greatly improved with a high extra computational complexity. The architectures are representative of many design styles and range from highly parallel architectures. Here a HWT-based reconfigurable system is designed using the EDK tool. Hardware architectures of a two dimensional have been implemented as a coprocessor in an embedded system. In addition, the hardware cost of this architectures is compared for benchmark images. This type of work using EDK can be extended to other applications of embedded system. Benefited from the effective optimization, a good image quality is achieved.

The future work will focus on improving the efficiency of the proposed algorithm but there is a Substantial gaps to compression limits still exist Trend toward algorithms to handle large, multidimensional images Trend to multiple core processors to spur development of new parallel processing paradigms Open question whether quantum information theory and quantum computation will save the day Here we have written the core processor Micro blaze is designed in system C Language, implemented using Xilinx platform studio and tested in SPARTAN-3 FPGA kit by interfacing a test circuit with the PC using the RS232 cable.

## V1.REFERENCES

[1].Q. Dai, X. Chen, and C. Lin,"A Novel VLSI Architecture for Multidimensional Discrete Wavelet Transform,"IEEE Transactions on Circuits and Systems for Video Technology, Vol. 14, No. 8, pp. 1105-1110, Aug. 2004.

[2].C. Cheng and K. K. Parhi, "High-speed VLSI implementation of 2-D discrete wavelet transform," IEEE Trans. Signal Process., vol. 56, no. 1, pp. 393-403, Jan. 2008.

[3].B. K. Mohanty and P. K. Meher, "Memory-Efficient High-Speed Convolution based Generic Structure for Multilevel 2-D DWT."IEEE Transactions on Circuits and Systems for Video Technology, VOL. 23, NO. 2, pp. 353363, Feb. 2013.

[4].I. Daubechies and W. Sweledens, "Factoring wavelet transforms into lifting schemes," J. Fourier Anal. Appl., vol. 4, no. 3, pp. 247-269, 1998.

[5].C.T. Huang, P.C. Tseng, and L.-G. Chen, "Flipping structure: An efficient VLSI architecture for lifting-based discrete wavelet transform, "IEEE Trans. Signal Process., vol. 52, no. 4, pp. 1080-1089, Apr. 2004.

[6].C.-Y. Xiong, J.-W. Tian, and J. Liu, "A Note on Flipping Structure: An Efficient VLSI Architecture for Lifting-Based Discrete Wavelet Transform," IEEE Transactions on Signal Processing, Vol. 54, No. 5,pp. 1910-1916, MAY 2006

[7].C.-T. Huang, P.-C. Tseng, and L.-G. Chen, "Analysis and VLSI architecture for 1-D and 2-D discrete wavelet transform," IEEE Trans. Signal Process., vol. 53, no. 4, pp. 1575-1586, Apr. 2005.

[8].C.-C. Cheng, C.-T. Huang, C.-Y. Ching, C.-J. Chung, and L.-G. Chen, "Onchip memory optimization scheme for VLSI implementation of line based two dimensional discrete wavelet transform," IEEE Transactions on Circuits and Systems for Video Technology, vol. 17, no. 7, pp. 814-822, Jul. 2007.

[9].H.Y. Liao, M. K. Mandal, and B. F. Cockburn, "Efficient architectures for 1-D and 2-D lifting-based wavelet transforms," IEEE Transactions on Signal Processing, vol. 52, no. 5, pp. 1315-1326, May 2004.

[10].B.F. Wu and C.F. Chung, "A high-performance and memory-efficient pipeline architecture for the 5/3 and 9/7 discrete wavelet transform of JPEG2000 codec," IEEE Trans. Circuits System. Video Technology., vol. 15, no. 12, pp. 1615-1628, Dec. 2005.

[11].C.-Y. Xiong, J. Tian, and J. Liu, "Efficient architectures for two-dimensional discrete wavelet transform using lifting scheme," IEEE Transactions on Image Processing, vol. 16, no. 3, pp. 607-614, Mar.2007.

[12].W. Zhang, Z. Jiang, Z. Gao, and Y. Liu, "An efficient VLSI architecture for lifting-based discrete wavelet transform," IEEE Transactions on Circuits and Systems-II: Express Briefs, Vol. 59, No. 3, pp. 158-162, Mar. 2012.

[13].B. K. Mohanty and P. K. Meher, "Memory Efficient Modular VLSI Architecture for High throughput and Low-Latency Implementation of Multilevel Lifting 2-D DWT," IEEE Transactions on Signal Processing, Vol. 59, No. 5, pp. 2072-2084, May 2011.

[14].A.Darji, S. Agrawal, Ankit Oza, V. Sinha, A.Verma, S. N. Merchant and A. N. Chandorkar , "Dual-Scan Parallel Flipping Architecture for a Lifting-Based 2-D Discrete Wavelet Transform,"IEEE Transactions on Circuits and Systems-II: Express Briefs, Vol. 61, No. 6, pp. 433-437, Jun. 2014