Design of Low Noise Amplifier at ISM band for WBAN Applications

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***Abstract*— A very large part of the low noise amplifier is of the receiver and must ensure restricted control Amplification with correct balancing of impedance. The built circuit is capable of operating at a supply voltage of 0.5 V and the wireless body area network was planned for Applications that use CMOS 130 nm technology. The simulation outcomes of the proposed LNA indicate a power output 16.27 dB gain and a 1.7 dB noise figure, while Just 1.44 mW of power is dissipating. The layout depicts excellent feedback matching the coefficient of input reflection (S11) obtained as -27,71 dB. The recommended job with -0.87 dBm IIP33, there is also very strong linearity..**

Index Terms*— *Low Noise Amplifier (LNA), Source Degenerated Common Source LNA (SD-CLNA), Wireless Body Area Network, Noise Factor (NF), Forward Gain.

I. INTRODUCTION

The wireless body area network offers the most favorable solution for wearable medical devices. It is very crucial to have receiver with very low power consumption, while meeting the specification with enough margins [1]. Being the first block of a typical receiver, the low noise amplifier design includes trade-offs between impedance matching, noise figure, linearity, gain and power consumption [2]. A number of low noise amplifier circuit techniques like cascade [3], cascode [4], folded-cascode [5] and the current re-use [6] topologies have been reported in the literature. For cascade topology the power consumption is very high due to multi-stage structure. The current re-use topology involves a matching network to re-use the current which increases the complexity of the design. The cascode topology is widely used for narrowband LNA design [7]-[9]. It improves the isolation between output port and input port which improves the stability of the circuit. It also provides very good gain with very low power consumption. But cascode topology reduces the voltage headroom due to its architecture. Though the folded cascode design requires lesser voltage compared to cascode topology, it demands higher current flow due to multiple gain stages. In cascode topology, usually forward body biasing [7] is used to handle the issue of the voltage head room. But this technique increases the complexity of the design as it requires extra supply voltages. To solve this issue we have used low threshold voltage MOS devices, which allows us to use the casocde topology without using FBB technique. Also the PCSNIM technique [10] is used for our design to obtain simultaneous input and noise matching considering power consumption as the main constraint. The LC tank circuit is used as output matching circuit to lessen the effect of parasitic capacitance of the cascode device.

II. DESIGN AND ANALYSIS of CIRCUIT

Due to its benefits such as impedance matching, isolation, gain and stability, Cascode is a generally accepted topology for low noise amplifier design. The source degenerated general source low noise amplifier (SD-CLNA) is the actual topology considered. The standard SD-CLNA topology schematic is shown in Fig. 1. At very low drain current[1], the SD-CLNA circuit is well known for its optimised noise efficiency with good gain. The typical SD-CLNA technique requires two inductors for simultaneous input and noise matching [11] as depicted in Fig. 1.

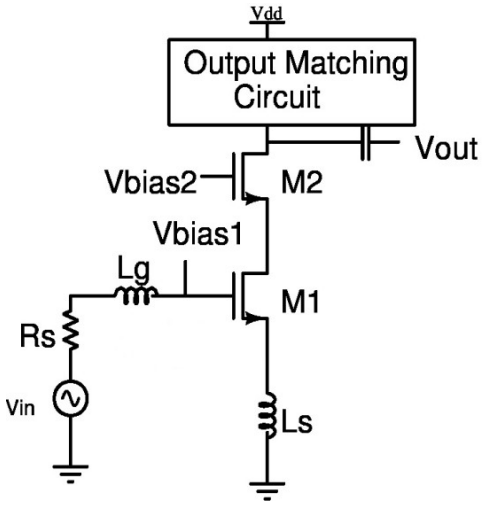

Fig 1. Typical circuit of the SD-CLNA

In conventional SDCLNA it is not possible to obtain a very good impedance matching at optimum noise and power [7]. Different optimization techniques have been reported in the literature [10-13] to solve this issue. The most popular one is power constrained input and noise matching where an capacitor (C_{ext}) is added between gate and source terminal of the common source device.

The proposed circuit including the bias circuit and output matching circuit is shown in Fig. 2. Input matching network consists of the gate inductor L_g, source inductor L, and the capacitor C. The capacitor C_{ext} along with good matching helps in reducing the value of the source inductor [14]. M1 performs as a common source device and M2 as cascode device. The input device is biased in the saturation region using the current mirror as demonstrated in Fig. 2. The size of the input transistor determines the optimum noise match [15]. The cascode configuration reduces the impact of gate-drain overlap capacitance which helps in decoupling the input and output port and improves the output impedance [16]. An LC tank circuit has been used as the output matching network. The output tank circuit along with resonating at the designed frequency help in reducing the parasitic effect of the cascode device.

In order to provide useful insight in the proposed circuit, theoretical analysis is provided regarding input matching technique and noise effect. Analyzing the small signal model of the input device (Fig. 3) the input impedance of the SD-CLNA is given as [1]

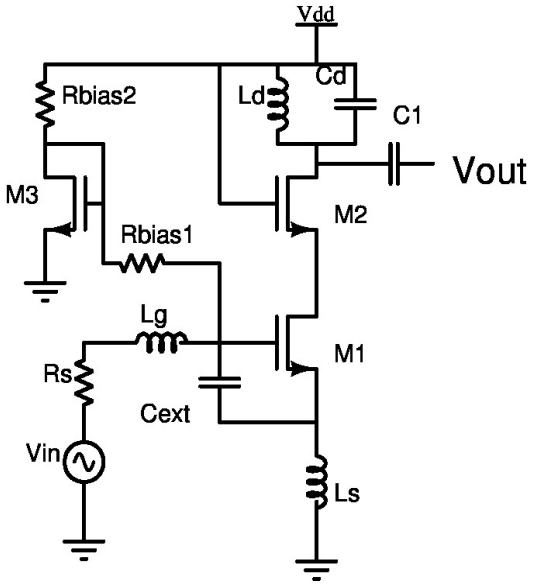

Fig 2. The proposed LNA circuit

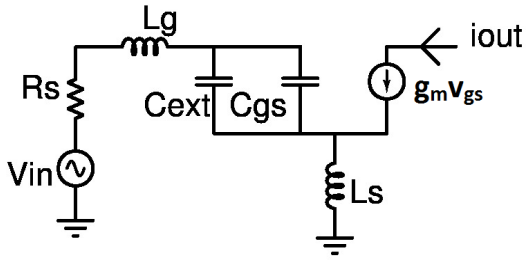

Fig. 3. Small signal equivalent circuitl of the input stage

The resonant frequency value is calculated from (1) as

$$\omega_0 = \frac{1}{\sqrt{L_t + C_t}} \quad (2)$$

Where,

$$L_t = L_g + L_s \quad (3)$$

And

$$C_t = C_{gs} + C_{ext} \quad (4)$$

It is clear from the above equations that at resonant frequency the input impedance is pure resistive in nature and the value of the input impedance is calculated as $(g_m L_s \mid C_t)$

Being the first block of receiver, it is very crucial for low noise amplifier to achieve a low noise factor. As the noise power of MOSFETs are greater than that of the inductors and capacitors, the capacitor and the inductor noise is ignored for simplicity [17]. The small signal model of the input stage considering noise sources is shown in Fig. 4. $\overline{i^2_{nd}}$ is expressed as [18]

$$\overline{i^2_{nd}} = 4kT\gamma g_{d0} \Delta f \quad (5)$$

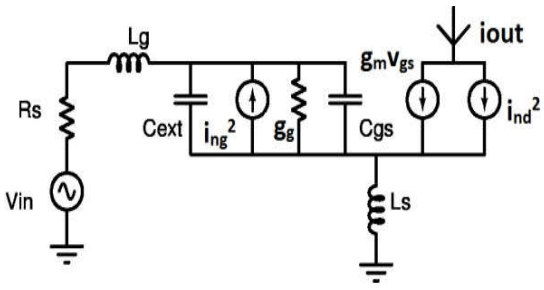

Fig. 4 Small signal equivalent circuit for noise analysis

Where g_{d0} is the drain to source conductance at Zero Vds and Δf is the bandwidth. The value of γ is 2/3 for long channel devices and more than 2 for short channel MOSFETs. The fluctuating channel potential couples with the gate terminal and results into noisy current. The mean squared value of the noisy gate current is expressed as [18]

$$\overline{i_{ng}^2} = 4kT\delta_{eff}\frac{\omega^2 C_t^2}{5g_{d0}}\Delta f \quad (6)$$

Where $\delta_{eff} = \delta\left(C_{gs}^2 / C_t^2\right)$ and the value of δ is 4/3. The noise factor of the SD-CLNA is expressed as [3]

$$NF = 1+\gamma g_m R_S\left(\frac{\omega}{g_m}\left(C_{gs}+C_{ext}\right)\right)^2 = 1+\frac{R_S\omega^2\left(C_{gs}+C_{ext}\right)^2}{g_m} \quad (7)$$

So it can be referred from the above expression that the value of the transconductance need to be very high to ensure lower value of the noise factor.

III. Simulation Results and Discussions

The designed low noise amplifier is implemented with 130nm RF-CMOS technology for 2.4 GHz applictions at a supply voltage of 0.5 V. the simulation work is carried out in cadence virtuoso environment. As shown in Fig. 5, the LNA shows the forward gain of 16.27 dB and reverse gain of -33.45 dB at 2.4 GHz. The design shows very good input matching with the value of S11 obtained as -27.71 dB as depicted in Fig. 6. The value of the output reflection co-efficient is -15.33 dB. The plot regarding NF and NFmin is given in Fig. 7.

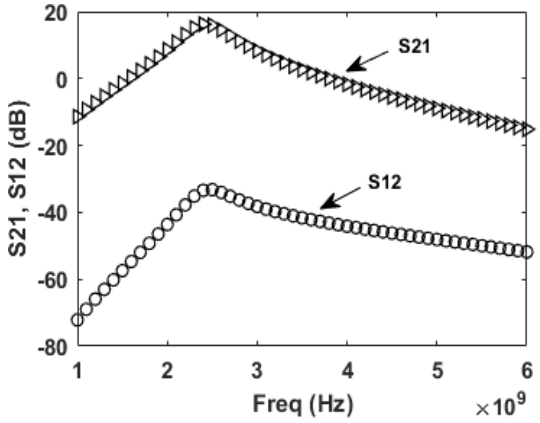

Fig. 5 The extracted result for S21 and S12

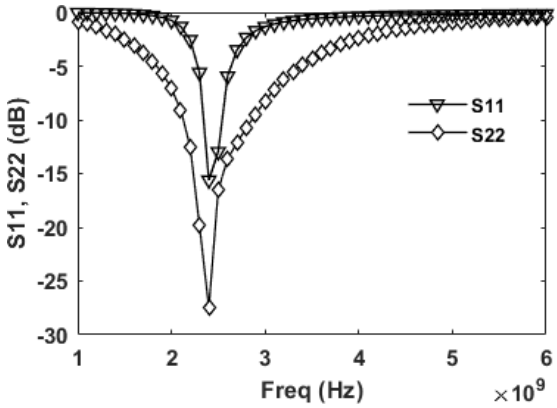

Fig. 6 The post layout simulation results of S_{11} and S_{22}

It can be noticed from the figure that the value of the NF is 1.7 dB which is very close to the minimum NF achievable for the designed circuit. A two–tone IIP3 simulation is performed using periodic steady state (PSS) analysis, to assess the linearity of the designed circuit. The output power corresponding to the operating frequency is shown in Fig. 8. The value of the IIP3 is obtained as -0.87 dBm, which signifies excellent linearity for the designed circuit. The power consumption of the designed circuit is 1.44 mW as demonstrated in Fig. 9.

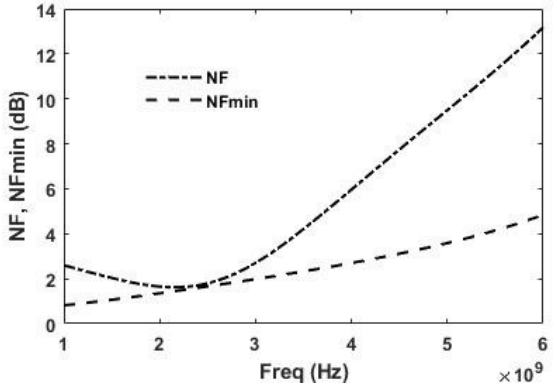

Fig. 7 NF and NFmin for the designed circuit

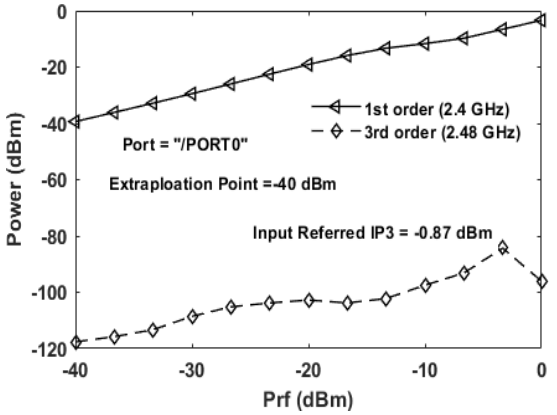

Fig. 8 IIP3 result considering 2.4 GHz as the fundamental frequency and 2.48 GHz as the third order frequency

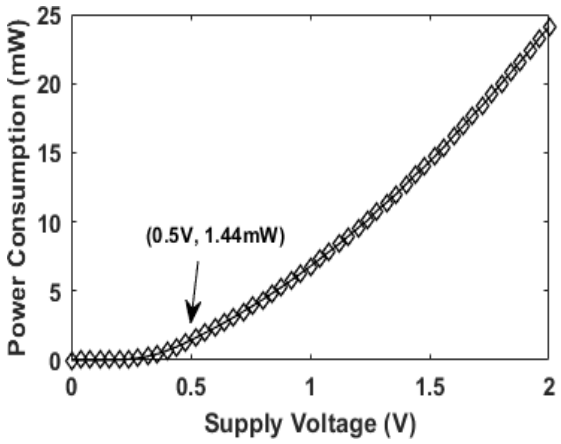

Fig. 9 the power consumption of the designed circuit

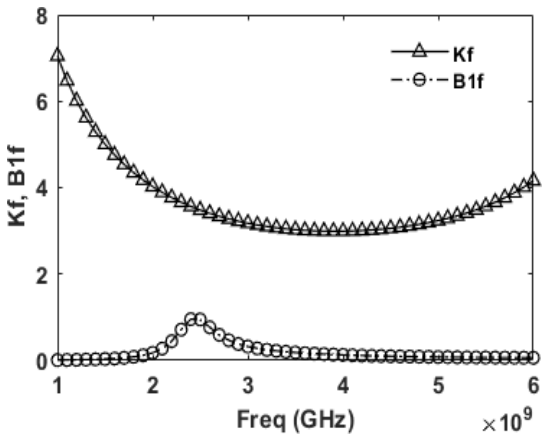

Fig. 10 the stability factors of the designed LNA

The plots regarding stability of the designed circuit is shown in Fig. 10.It is noticed, that the value of K_f is greater than 1 and the value for B_{1f} is less than 1 which signifies unconditional stability for the designed circuit.

The physical design of the designed circuit is depicted in Fig. 11. MIM (metal-insulator-metal) capacitor and poly resistor are used in the design as they have less variations with respect to process and temperature. The top metal is used as the ground as it has the least resistivity among all the metal options. A performance comparison has been shown in table 1 to validate our design with respect to the existing work reported in the literature.

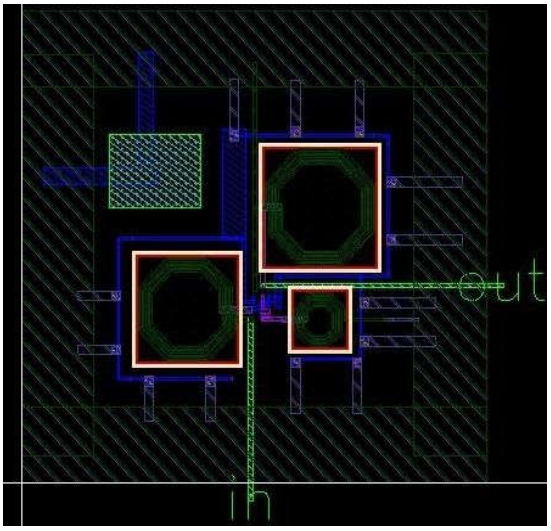

Fig. 11 The physical design of the proposed LNA

CONCLUSION

In this work a LNA is proposed to work at a supply voltage of 0.5V without using forward body biasing. The LNA shows very good gain of 16.27 dB, while dissipating only 1.44 mW of power. The reverse voltage gain is obtained as -33.45 dB, which signifies very good isolation between output and input port. The designed circuit also shows very good linearity along with very low NF of 1.7 dB. The proposed circuit is unconditionally stable for the designed frequency.

TABLE I. PERFORMANCE COMPARISON WITH THE EXISTING WORK IN THE LITERATURE

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Parameters	This Work	[6]	[18]	[19]	[20]	[21]	[22]	[23]	[24]
Freq (GHz)	2.4	2.4	2.4	2.4	3.5	2.4	2.4	5	5.2
Vdd (V)	0.5	0.5	0.5	1		1	0.6	0.6	0.6
Pdc (mW)	1.44	2.1	1.5	0.98	6.5	12	3	1.3	1.1
Gain (dB)	16.27	18.7	14.13	15.2	11	15	15	12.5	10
S11 (dB)	-27.72				-12				
IIP3 (dBm)	-0.87	-4.9		-19	-9		-7	-2	-8.6
NF (dB)	1.7	1.5	2	5.2	4.6	2	3	3.5	3.7

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