HIGH SPEED SYNCHRONIZATION OF INTERCONNECT TRANSCEIVERS USING DELAY LOCKED LOOP (DLL)

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ABSTRACT: In this paper a novel architecture for an ADL is presented. The design employs a digital tapped delay line and a fully digital phase detector and controller. The design is fully digital and uses only standard static logic gates. The design does not include analog components nor does it use digital components belonging to other logic families. A multi-controlled delay cell for the voltage-controlled delay line is applied to provide the wide operating frequency range and low-jitter performance. The charge pump circuit is implemented using a digital control scheme to achieve adaptive bandwidth. The design is based on dividing the DLL circuit into independent groups of taps for optimum tap selection. A simple technique to phase blend a DDL with phase difference in coarse step improves the coarse time resolution without additional lock time. Based on this improved time resolution, the further step can be completed to provide fast lock time, high accuracy and low power consumption. At last compared to existed system, proposed system gives effective results in terms of power, delay and speed of operation.

KEY WORDS: Delay-locked loop, mixed-mode, fast locking, phase blend, dual delay line, time-to digital converter, low power.

I.INTRODUCTION

Nowadays, DLLs and PLL (Phase locked loop) s are widely used in memory devices, high-speed microprocessors and communication integrated circuits. In these applications, the signal skews and jitters are removed using the DLL or PLL for high-speed signalling. PLL has the advantage of providing the input frequency at various output frequencies. However, the PLL suffers from long locking time.

As an alternative to these PLLs, DLLs have been considered because they are more stable, easier to implement with digital circuits, And provide better jitter performance. Generally, if no frequency multiplication is required, DLLs are more attractive than PLLs because they are more stable and easier to implement with digital circuits. They also exhibit better jitter accumulation characteristics than PLLs.

DLLs can generally be classified into three types: analog, digital, and mixed mode. Analog DLL have better skew and jitter. However, it is not widely used these days because of analog DLL process variability, which is more affected and has a high degree of integration due to long locking time and large area. As an alternative to these analog DLLs, digital DLLs can be easily shrunk and have a faster locking time. An open-loop digital DLL has the fastest locking time and low power consumption. However, it has low accuracy and low immunity, compared with closed-loop type, due to PVT (Process, Voltage and Temperature) variations. Many designers have suggested several ways to overcome these.

To accelerate the lock time in closed-loop, the two-stage TDC digital DLL, with coarse step and fine step, uses a relatively fast lock time and closed loop. PVT variations can be compensated for. However, the digital DLL is good, but there is a phase error and the jitter increases by DNL due to the dithering that occurs in closed loop. If there is a false lock error in the coarse lock step, the control circuit is used to resolve the false

lock error. Maintain 1 clock cycle latency to solve the problem. However, such a DLL may be caused by such a complex circuit, leading to increased area, increased power consumption, and poor performance. Mixed-mode DLL does not degrade relatively small jitter performance compared to digital DLLs, but with relatively small area and power overhead.

In the coarse lock step, the frequency range is selected by TDC method to improve time resolution. Based on the narrowed frequency range, the VCDL (voltage control delay line) is adjusted with an analog feedback loop that is a fine step to provide relatively fast lock times. Mixed-mode DLLs offer low jitter by implementing precise digital-to-digital control and the advantage of being able to compensate for PVT variations. However, this locking time is still long. A high-performance DLL with both low jitter and fast locking time is required. Low-jitter is provided using a coarse-grained TDC scheme and an accurate analog feedback loop. To achieve fast lock times versus conventional DLL, we propose a mixed-mode DLL that improves resolution by phase blending DDL (dual delay lines) at coarse step.

Conventional DLLs may suffer from harmonic locking over a wide operating frequency range. Therefore, various wide-range DLLs architectures have been developed to solve the false locking problem. DLLs with dual-loop architectures is presented to overcome the problem of a limited delay range using multiple VCDLs. In, an all-analog DLL uses the replica delay line to solve the narrow operating frequency-range problem of a conventional DLL. However, the analog DLLs are more strongly affected by the process variation. Therefore, digital DLLs is developed to improve process portability. In the all-digital multiphase clock generator is used to overcome the false locking problem. In phase selector circuit and start-controlled circuit are used to solve false locking problems and maintain the latency of one clock cycle.

II. EXISTED SYSTEM

The below figure (1) shows the block architecture of existed system. Basically, it requires two input signals as shown in figure (1). DLLs have been used for clock distribution circuits, multiphase clock generation and clock recovery circuits. These two inputs are used in clock recovery circuits. The first type of DLL is used in our applications as it is suitable for synchronous interconnect circuit. The DLL's loop can be analysed with continuous time. The approximation of this system is as long as lower limit of bandwidth below the operating frequency.

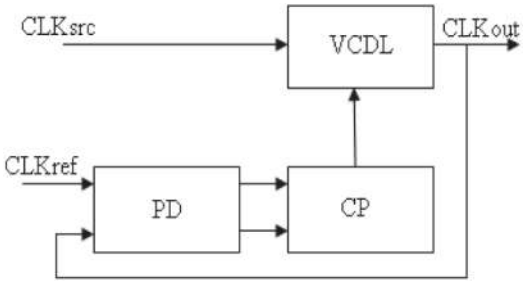

Fig. 1. Existed system

The delay line is tapped at every other inverter output. In this the delay line receives a local clock signal and passes it through a series of delay line taps. Phase adjustment is performed by selecting suitable taps of the delay line. Each tap provides a signal adjacent in phase to the signal at its neighbouring taps and shifted from the previous tap by two inverters delay. The length of the delay line depends on the frequency of the input data and the inverter delay.The physical layout of existed system is shown in below figure (2). In this there is no need of linear regulator at the output to drive the control voltage.

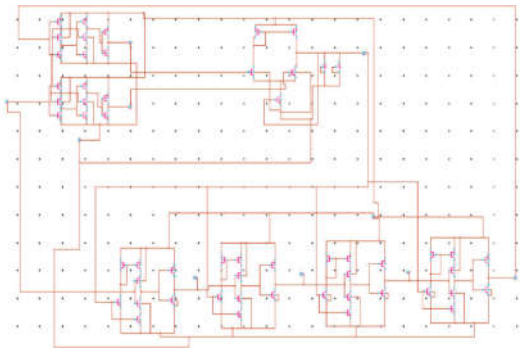

Fig. 3. Layout of Existed system

When a new edge occurs, the circuit does not switch to the new tap but continues sampling DATA_IN with the old tap and prepare the new tap. This means that the two taps are needed simultaneously until switching takes place. The difference between two selected phases is one buffer delay. After the coarse lock is completed, the two selected phases pass through the phase blender and output. However, this method is accompanied by a large area that is suffering from long-term dead time, large power loss, production of analogue intensive, large-capacity and extensive calibration required. In the same time resolution of the circuit increases, due to this delay increases. To decrease the delay occurred in the system a new system is proposed which is discussed in below section.

III. PROPOSED SYSTEM

The purpose of this DLL is to provide an output clock signal very close in phase to the data edges. The main feature of the proposed design is implementing a priority selector circuit for optimum tap selection with a reduced number of gates and propagation delay. The idea is based on dividing the circuit into independent groups, which can be activated or deactivated by a priority selector. The below figure (4) shows the physical layout of proposed system. The first stage of proposed system consists of 16 phase output. In the case of a coarse step using a conventional inverter is composed of a 16-buffer stage. Each buffer stage is composed of two tri-state inverters in the same manner as the resolution of the DDL.

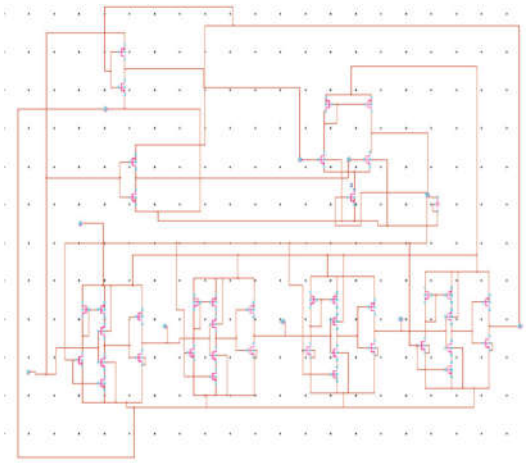

Fig. 4. Layout of Proposed system

Each phase is output based on the delay of two tri-state inverters. Here DLL is composed at the front of the delay line to enable fine delay. The proposed DLL improves the time resolution of the inverter by a factor of two in two clock cycles at the coarse step. During the course step of the two clocks, two of the 16 phases are selected and applied to the DDL. At this time, the difference between two selected phases is one buffer delay. Many designers have suggested several ways to improve the resolution. Both positive and negative transition edges of a clock are used to implement the DLL.

It has the advantage of implementing half of the resolution compared to the conventional DLL. To implement this DLL, a dual delay lines and a large area symmetric flip flops should be used and an edge combiner is required. When the reference clock duty is changed by more than a certain amount, it is vulnerable due to difference of positive and negative transition edges of a clock.These methods address the limitation of coarse intrinsic delay of buffer elements and apply the gate

delay is to improve the resolution below the sub-gate delay.

Table. 1. Performance comparison

S.NO	Specification	Proposed system	Existed system
1	Locking time	4	6
2	Jitter	~2.3 ps @2.8GHz	~ 8ps @ 1.2 MHz
3	Operating frequency	650-3 GHz	650-1.25 MHz
4	Transistor Count in Phase Detector	2	8
5	Transistor Count in Charge Pump	5	7

The below figure (5)shows the output of proposed system.

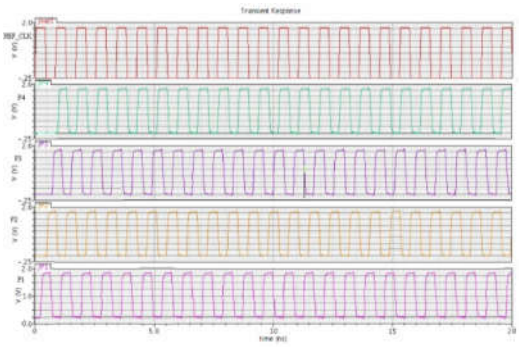

Fig. 5. Output waveform of proposed system

Our proposed DDL scheme can be implemented simply and without the need for additional clock, large area or high power consumption. Due to the coarse step, the voltage range to be controlled can be reduced due to the narrowed time resolution in the analog loop, which is a fine step. Since the phase out clock must cover both the fast and slow states relative to the reference clock, charge the initial state of the capacitor of the loop filter to half of supply voltage and finish the analog step at a fast lock time. Therefore, the maximum correction time of the proposed DLL is within less number of clock cycles. From below table 1 we can observe the performance comparison of existed and proposed system.

IV. CONCLUSION

The DLL proposed in this paper provides fast lock time, high accuracy and low power consumption. To achieve these, we have a simple technique of DDL with phase difference in the first coarse step, which improves the coarse step time resolution without additional lock time. The coarse tune circuit is proposed to reduce the lock time and keep a better jitter performance in this DLL. The charge pump circuit is implemented by the digital control scheme to achieve adaptive bandwidth. Consequently, this DLL can operate correctly when the input clock frequency is changed. With this improved system, we can achieve a faster locking time by performing the second fine analog step.

V. REFERENCES

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